

REMARKS

As a preliminary matter, applicants appreciate the courtesy extended to Patrick Burns and Matthew Hitching in an interview on April 26, 2005. The substance of the interview is adequately described in the Examiner's Interview Summary mailed May 4, 2005.

Applicants also appreciate the review of two proposals given to the examiner informally after the interview. On about May 17, 2005, the examiner indicated that either of the proposals alone might overcome the outstanding rejection and that the combination of the two proposals also might overcome the rejection. No agreement was reached.

The two proposals previously made have not been combined in this response. Applicants believe that the claims are allowable over the references of record for the following reasons.

Independent claims 1, 14, 15 and 30 have been amended to better define a "common opcode bit" in the claims. According to the definition in the amended independent claims "each said opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of external formats F1 and F2 is a common F1-F2 opcode bit in the format concerned". The qualification "F1-F2" has been added in view of a different kind of common opcode bit introduced in dependent claim 3.

The definition of the common opcode bits in the amended independent claims also specifies that "each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$ ".

In the office action of February 23, 2005, the Examiner indicated in paragraph 25 that she interpreted the former definition of the common opcode bits as permitting the reader to choose just one of the common opcode bits, even if there are actually several common opcode bits, because the original definition referred to “at least one ...”. It is believed that this possible interpretation is excluded in the new definition, which says that *each* opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of the external formats F1 and F2 is a common F1-F2 opcode bit.

With the new definition of the common opcode bits, each of the independent claims 1, 14, 15 and 30 is believed to be patentably distinguishable from the Kissell reference (“MIPS 16: high-density MIPS for the embedded market”) as interpreted in the light of the further reference “Product Description: MIPS application-specific extension”. As the Product Description document shows, the opcode bits in the MIPS 16 instruction are the bits 11 through 15. In the 32-bit MIPS instruction the opcode bits are bits 26 through 31. The opcode bits of the MIPS 16 instruction are all in different bit positions from the opcode bits in the 32-bit MIPS instruction. Thus, it appears that the opcode bits in the MIPS 16 format and the 32-bit MIPS format are not “common opcode bits” in the sense required by the amended independent claims.

To qualify as a common opcode bit in the sense of amended independent claims 1, 14, 15 and 30, an opcode bit in the MIPS 16 format must have an individually corresponding opcode bit in the 32-bit MIPS format. For example, as explained in the first Office Action, taking the number C of common opcode bits to be 5, the common opcode bits

in the 32-bit MIPS instruction could be chosen as the bits 26, 27, 28, 30 and 31. All of the opcode bits 11 through 15 in the MIPS 16 format would be common opcode bits. This seems a reasonable assumption since the LB instruction in the 32-bit format could be formed by taking the 5 opcode bits (“10000”) from 11 through 15 in the LB MIPS 16 instruction, mapping them respectively to bits 26, 27, 28, 30 and 31, and setting bit 29 to “0”. This produces, as bits 26 through 31 of the 32-bit MIPS instruction, “100000” which according to the Product Description document is the opcode for LB in the 32-bit MIPS format.

This mode of translation would even work for the subsequent LBU, LH, LHU and LW instructions. However, it breaks down for other subsequent instructions in the Product Description, for example the Store Byte instruction SB shown on page 32 of the Product Description reference. In this case, the translation of the SB MIPS 16 instruction (“11000”) produces the opcode “110000”, whereas the correct opcode for the SB 32-bit MIPS instruction is “101000” as shown on page 32 of the Product Description reference. In this case, bit 27 (which was assumed to correspond to bit 12) is “0” whereas bit 12 is “1”, and bit 28 (which was assumed to correspond to bit 13) is “1” whereas bit 13 is “0”. In other words, not all the mutually-corresponding opcode bits are identical to one another. It is believed that, whatever choice of common opcode bits is made in the Product Description reference, the requirement of the amended independent claims for *all* the mutually-corresponding common opcode bits in the two external formats to be identical to one another is not met for *every* available first operation.

As noted in our response to the first Office Action, the significance of this is

that in the MIPS processor the conversion from MIPS 16 format into 32-bit MIPS format cannot be independent of the operation specified by the external format instruction. In other words, a different translation operation is required for the SB operation compared to the LB operation. Accordingly, the instruction translation unit in the MIPS processor is more complicated and hence either functions more slowly or utilizes more computational resources than the instruction translation unit in the present invention. For example, it appears that the instruction translation unit in the MIPS processor may have to partially decode the instruction to translate it and/or may need to use some form of look-up table. In the present invention, on the other hand, because the common opcode bits are identical for every first operation, no such decoding or look-up table is necessary.

Claim 3 has been amended for consistency with amended claim 1. This claim introduces “common F2-F3 opcode bits” which are common to the second and third formats F2 and F3. An opcode bit in format F2 may be a common F2-F3 opcode bit as well as a common F1-F2 opcode bit, as is the case for each of the three opcode bits in positions $i+1$, $i+2$ and $i+3$ in format F2 in the example of Figure 3(B) of the present application.


Claim 32 is a new independent claim, also directed to a processor embodying the present invention. This claim does not define “common opcode bits”. Instead, this claim defines a “common bit position”. Each bit position at which the first and second external formats both have respective opcode bits is a common bit position within the meaning of new claim 32. For example, in the example of Figure 3(B) of the present application, the common bit positions for the formats F1 and F2 are the bit positions $i+1$, $i+2$ and $i+3$. This definition

of the invention is clear and succinct in the case of a processor in which the “common opcode bits” in the two external formats have the same bit positions. However, this definition is inapplicable to a processor such as the MIPS processor discussed above, in which the potential common opcode bits are at different bit positions in the two formats under consideration, for example the positions 11 through 15 in the MIPS 16 format and the positions 26 through 31 in the 32-bit MIPS format. As will be apparent from the discussion above, the applicants intend to encompass with amended independent claims 1, 14, 15 and 30 the possibility that two mutually-corresponding opcode bits (one from format F1 and the other from format F2) may be in different bit positions in the two formats. In view of this, in new claim 31, the limitation that the common F1-F2 opcode bits have the same bit positions in the two formats is presented merely as an optional feature of the processor of claim 1.

For the foregoing reasons, applicants believe that this case is in condition for allowance, which is respectfully requested. The examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Patrick G. Burns
Registration No. 29,367

June 21, 2005

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315
Customer No. 24978
P:\DOCS\0808\65688\979847.DOC